MEMORY MODELING CIRCUIT WITH FAULT TOLERATION

BACKGROUND OF THE INVENTION

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1. Field of the Invention

This invention generally relates to the field of a design for a fault toleration circuit. More particularly, the present invention relates

10 to a memory modeling circuit with fault toleration.

2. Description of the Prior Art

Many devices require memory systems with high reliability,

15 such as servers in enterprises or government offices; mainframes in financial institutions; equipment in hospitals; navigation systems for aircrafts or spaceships; even the devices used in severe environments. The memory systems with high reliability are required in order to ensure the accuracy of data and make whole system work regularly

20 since the memory systems in those devices are used in storing important data.

In order to improve the reliability of memories, well-known methods are to add testing items to memories for picking those

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defected out before their leaving the factor; to disable or discard error bit and even to correct it by software detecting/debugging.

Although the reliability of memory can be effectively improved

5   in real time by software detecting/debugging, the only one way is to replace a new one while the data stored in the memory occurs numerous errors. As to other methods, they cannot detect error in real time but only compensation.

10   This is, one bit error or a few data errors can be processed in real time by adopting software detecting/debugging method. However, the whole system will shut down and lose the important data stored in memory while numerous data errors occur in the memory. As to other methods, they only can improve the product reliability in the future by

15   analyzing the historical errors but cannot deal with the error in real time.

Therefore, there is a need for providing a memory modeling circuit with fault toleration that can detect and correct error(s) in real

20   time.

SUMMARY OF THE INVENTION

In accordance with the present invention, a memory modeling

circuit with fault toleration is provided and substantially obviates one or more of the problems resulted from limitations and disadvantages of the prior art mentioned in the background.

5   Accordingly, one object of the present invention is to provide a memory modeling circuit with fault toleration for detecting and correcting the error(s) in a memory system.

Another object is to provide a memory modeling circuit with 10 fault toleration for detecting the faulty memory.

Still another object is to provide a memory modeling circuit with fault toleration for improving the reliability of a memory system.

15   According to the objects mentioned above, the present invention provides a memory modeling circuit with fault toleration, including: a compare circuit, a control circuit and a test circuit. The compare circuit receives the data stored in the same address of memories and compares data with each other to produce the correct 20 reading data. The control circuit connects with the control signals of memories and detects that control signals. The control circuit has data output/input ports. While the control signal of the memories is to write, the control circuit enters a writing mode and writes the writing data received from the data output/input ports in the same address of the

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memories. While the control signal of the memories is to read, the control circuit enters a reading mode, receiving the reading data generated by the compare circuit and outputs it through the data output/input ports. The test circuit receives the data stored in the same address of the memories and the reading data generated by the compare circuit to generate a testing result. The testing result can identify a faulty memory or a faulty compare circuit.

The compare circuit or the test circuit can include several sub-circuits with the same circuit design. Further, while the control circuit is in a writing mode, it stops receiving the data sent from the compare circuit until the control circuit enters a reading mode. While the control circuit is in a reading mode, it makes the compare circuit stop writing data to memories until the control circuit enters a writing mode.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. 1A illustrates a block diagram in accordance with the concept of the present invention;

FIG. 1B illustrates one preferred circuit embodiment of the
5   present invention;

FIG. 2A shows a logic circuit of the compare circuit in FIG. 1B;

FIG. 2B shows a logic truth table of the circuit in FIG. 2A;
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FIGS. 3A to 3D show the output results and the corresponding errors to the test circuit in FIG. 1B;

FIG. 4 shows a logic circuit of the test circuit in FIG. 1B;
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FIG. 5 shows a logic circuit of the control circuit in FIG. 1B; and

FIG. 6A and 6B illustrate a logic truth table and the status of
20   memory reading/writing for the circuit in FIG. 5.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Some preferred embodiments of the invention will now be

described in greater detail. Nevertheless, it should be noted that the present invention can be practiced in a wide range of other embodiments besides those explicitly described, and the scope of the present invention is expressly not limited except as specified in the

5   accompanying claims.

The present invention provides a memory modeling circuit with fault toleration, including: a compare circuit, a control circuit and a test circuit. The compare circuit receives the data stored in the same

10   address of memories and compares data with each other to produce the correct reading data. The control circuit connects with the control signals of the memories and detects that control signals. The control circuit has data output/input ports. While the control signal of the memories is to write, the control circuit enters a writing mode and

15   writes the writing data received from the data output/input ports in the same address of memories. While the control signal of the memories is to read, the control circuit enters a reading mode, receiving the reading data generated by the compare circuit and outputs it through the data output/input ports. The test circuit

20   receives the data stored in the same address of the memories and the reading data generated by the compare circuit to generate a testing result. The testing result can identify a faulty memory or a faulty compare circuit.

The compare circuit or the test circuit can include several sub-circuits with the same circuit design. Further, while the control circuit is in a writing mode, it stops receiving the data sent from the compare circuit until the control circuit enters a reading mode. While the control circuit is in a reading mode, it makes the compare circuit stop writing data to memories until the control circuit enters a writing mode.

FIG. 1A illustrates the concept of the present invention. While data will be written to the memory 10, the control circuit 40 receives the writing data and writes it to the same address of the first memory 100, the second memory 102 and the third memory 104 at the same time. While data will be read from the memory 10, the reading data is read from the same address of the first memory 100, the second memory 102 and the third memory 104, being sent to the compare circuit 20 to compare with each other to ensure the accuracy of itself, and is outputted through the control circuit 40.

The present invention further discloses that the test circuit 30 simultaneously receives the data from the memory 10 and the compare circuit 20 in order to identify the fault part among the first memory 100, the second memory 102, the third memory 104 and the compare circuit 20 while any fault occurs in the reading process.

FIG. 1B illustrates one preferred embodiment of the present invention. The first memory 100, the second memory 102 and the third memory 104 use the same type of memory and simultaneously store the same data. In the present preferred embodiment, the first memory 100, the second memory 102 and the third memory 104 use the synchronous dynamic random access memory (SDRAM). The output/input ports DQ0 of the first memory 100, the second memory 102 and the third memory 104 are respectively connected with the input ports I1, I2 and I3 of the first compare circuit, as shown in FIG. 1B.

The data stored in the first memory 100, the second memory 102 and the third memory 104, theoretically, should be the same while there is no any fault. The first compare circuit 106 compares with the data sent from the output/input ports DQ0 of the memories. For example, assuming the correct data of the three output/input ports DQ0 is "1". While all output data are "1" or any two of them are "1", the correct output "1" still can be gotten through the operation of the first compare circuit 106. This is, the compare circuit of the present invention can detect and tolerate a faulty memory. This means the correct output data can be gotten through the compare circuit unless two faults occur simultaneously on the output/input ports DQ0 among the first memory 100, the second memory 102 and the third memory 104.

Similarly, the output/input ports DQ1 of the first memory 100, the second memory 102 and the third memory 104 are respectively connected with the input ports I4, I5 and I6 of the second compare circuit; the output/input ports DQ2 are respectively connected with the input ports I7, I8 and I9 of the third compare circuit; the output/input ports DQ3 are respectively connected with the input ports IA, IB and IC of the fourth compare circuit, as shown in FIG. 1B.

FIG. 2A shows a circuit diagram of the compare circuit described above, and FIG. 2B shows the logic truth table of the compare circuit in FIG. 2A. However, the compare circuit in FIG. 2A is one preferred circuit for the present embodiment, and other logic circuits to produce the result of the truth table in FIG. 2B also can be applied to other embodiments.

Furthermore, the present invention can not only detect and correct the fault data but also identify the faulty memory or compare circuit in order to let an engineer repair the fault part in real time to keep the reliability of memory system.

Referring to FIG. 1B again, the first test circuit 114 has four input ports respectively connected with three input ports I1, I2, and I3, and one output port OA of the previous stage first compare circuit 106,

and has output ports named from C0 to C5. While the outputs as shown in FIG. 3A respectively appear on the ports C0 to C5 of the first test circuit 114, the faulty memory or compare circuit can be identified. For example, while the output ports C0 to C5 of the first test circuit 114 are "C0=1, C1=0, C2=0, C3=1, C4=1, C5=0", the output port DQ0 (I2) of the second memory 102 is fault according to FIG. 3A. Another example, while the output ports C0 to C5 of the first test circuit 114 are "C0=0, C1=0, C2=1, C3=0, C4=1, C5=1", the output port 0A of the compare circuit 106 is fault according to FIG. 3A.

Similarly, the second test circuit 116 has four input ports respectively connected with three input ports I4, I5, and I6, and one output port 1A of the second compare circuit 108, and has output ports named from C6 to CB. The third test circuit 118 has four input ports respectively connected with three input ports I7, I8, and I9, and one output port 2A of the second compare circuit 110, and has output ports named from CC to CH. The fourth test circuit 120 has four input ports respectively connected with three input ports IA, IB, and IC, and one output port 3A of the fourth compare circuit 112, and has output ports named from CI to CN. Moreover, the same method as described in the first test circuit 114, the faulty memory or compare circuit can be identified according to the outputs of the second test circuit 116, the third test circuit 118 and the fourth test circuit 120. FIG. 4 shows a preferred logic circuit embodiment of the test circuit in FIG. 1B.

Referring to FIG. 1B again, since reading from or writing to memory is through the same ports, such as the data read from or written to the first memory 100 is through the same ports DQ0~DQ3, the first control circuit 122, the second control circuit 124, the third control circuit 126 and the fourth control circuit 128 are used in controlling the output/input ports of the respective memory in reading mode or writing mode.

For example, while the memories is in a writing mode, the statuses of the control signal ports T0 to T3 respectively are 1CS(T0)=0, 1CAS(T1)=0, 1RAS(T2)=1 and 1WE(T3)=0. At this moment, the first control circuit 122 senses the memories in the writing mode through its ports, T0, T1, T2 and T3, connected with the ports, T0, T1, T2 and T3, of the control signal ports of the memories, hence the first control circuit 122 enters the writing mode. Moreover, while the first control circuit 122 is in the writing mode, the port F0 is used in receiving writing data and respectively connecting with the ports DQ0 of the first memory 100, the second memory 102 and the third memory 104 through the ports, I1, I2 and I3, of the first control circuit 122 in order to write the data of the port F0 to the memories. As shown in FIG. 1B, the port I0A of the first control circuit 122 is connected with the port 0A of the first compare circuit to get the correct output data through the compare circuit. However, while the first control circuit is in a

writing mode, the port I0A will be disabled from receiving data firstly.

On the other hand, while the memories is in a reading mode, the statuses of the control signal ports T0 to T3 respectively are 1CS(T0)=0, 1CAS(T1)=0, 1RAS(T2)=1 and 1WE(T3)=1, and the first control circuit 122 is switched to the reading mode. At this moment, the port I0A of the first control circuit 122 receives reading data from the port 0A of the first compare circuit and outputs the data through the port F0 of the first control circuit 122. The ports, I1, I2 and I3, will be disabled while the first control circuit is in a reading mode.

As described above, while the ports, F0, F1, F2 and F3, of the first control circuit 122, the second control circuit 124, the third control circuit 126 and the fourth control circuit 128 are used in receiving writing data, the control circuits disable the ports I0A, I1A, I2A, I3A and respectively connect with the ports DQ0, DQ1, DQ2 and DQ3 of the memories through the ports I1, I2, I3, I4, I5, I6, I7, I8, I9, IA, IB and IC, to write data into the memories, as shown in FIG. 1B. While the ports, F0, F1, F2 and F3 are used in receiving reading data, the control circuits disable the ports I1, I2, I3, I4, I5, I6, I7, I8, I9, IA, IB and IC, receiving the correct data at the ports I0A, I1A, I2A, I3A from the compare circuits and output the reading data through the ports F0, F1, F2 and F3 of the control circuits.

FIG. 5 shows a logic circuit example of the control circuit in accordance with the present invention. FIG. 6A and 6B show the logic truth table of the control circuit in FIG. 5, and the statuses of memory reading/writing. As shown in FIG. 5, as X=1 and Y=0, the control circuit enters a reading mode. P2 and P3 are turned off but P0 and P1 are turned on to make the connection point P be "1". Q0 and Q1 are turned off but Q2 and Q3 are turned on to make the connection point Q be "0". Hence, the left side of the K is "0" and the left side of the L is "1" to make the N turn off but the M turn on. While the status of X=0 and Y=0 in reading data process, Q1 and Q2 are turned off to make the voltage of the connection point Q retain in the status of X=1 and Y=0 so that the left side of the L is still "1"; also, P0 and P3 are turned off to make the voltage of the connection point P retain in the status of X=1 and Y=0 so that the left side of the K is still "0". The reading mode is still hold by the control circuits until the status is changed to X=0 and Y=1. Meanwhile, P2 and P3 are turned on but P0 and P1 are turned off so that the connection point P is "0"; also, Q0 and Q1 are turned on but Q2 and Q3 are turned off so that the connection point Q is "1". This makes the left side of the K is "1" and the left side of the L is "0". This makes the N be turned on but the M be turned off. While the status of X=0 and Y=0 occurs in writing mode, Q1 and Q2 are turned off to make the voltage of the connection point Q retain in the status of X=0 and Y=1 so that the left side of the L is "0"; also, P0 and P3 are turned off to make the voltage of the connection point P retain in the

status of X=0 and Y=1 so that the left side of the K is "1". This makes the writing mode is hold by the control circuits until the next change.

5   Although specific embodiments have been illustrated and described, it will be obvious to those skilled in the art that various modifications may be made without departing from what is intended to be limited solely by the appended claims.